CLAIMS:

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

a film stack formed on the semiconductor substrate and including a tunable anti-reflective coating formed within said film stack having a structural formula R:C:H:X, wherein R is selected from the group consisting of Si, Ge, B, Sn, Fe, Ti, and combinations thereof, and wherein X is not present or is selected from the group consisting of one or more of O, N, S, and F; and

a damascene structure for a metal interconnect formed in the film stack.

2. The device of claim 1, wherein said tunable anti-reflective coating comprises a part of a lithographic structure during the formation of said metal interconnect in said film stack.

3. The device of claim 1, wherein said tunable anti-reflective coating comprises a chemical mechanical polishing (CMP) stop layer for said damascene structure.

4. The device of claim 1, wherein said tunable anti-reflective coating comprises at least one of a single hard mask, a top layer in a multiple layer hard mask, and an anti-reflective coating.

5. The device of claim 1, wherein said tunable anti-reflective coating is configured to have optical properties that substantially match the optical properties of said film stack.

6. The device of claim 5, wherein said optical properties comprise at least one of an index of refraction, and an extinction coefficient.

7. The device of claim 6, wherein said index of refraction comprises a value ranging from 1.4 to 2.6.

8. The device of claim 6, wherein said extinction coefficient comprises a value ranging from 0.01 to 0.78.

9. The device of claim 6, wherein at least one of said index of refraction and said extinction coefficient is graded along a thickness of said tunable anti-reflective coating.

10. The device of claim 6, wherein said index of refraction comprises a value ranging from 1.2 to 2.6.

11. The device of claim 1, wherein said tunable anti-reflective coating comprises at least one of chemical vapor deposition (CVD) coating, and plasma enhanced CVD coating.

12. The device of claim 1, wherein said tunable anti-reflective coating is configured to provide at least one of control of a critical dimension of said single damascene structure, and control of a critical dimension variation of said damascene structure.

13. The semiconductor device of claim 1, wherein said damascene structure is a single damascene structure.

14. The semiconductor device of claim 1, wherein said damascene structure is a dual damascene structure.

15. The semiconductor device of Claim 1, wherein said film stack further comprises a low-k dielectric layer.

16. A process for forming an integrated circuit structure comprising:

forming a layer of dielectric material on a substrate;

forming a layer of tunable etch resistant anti-reflective (TERA) material on said layer of dielectric material; and

forming a damascene structure for a metal interconnect by using said layer of TERA material as at least one of a lithographic structure for the formation of the interconnect structure, a hard mask, an anti-reflective coating, and a chemical mechanical polishing (CMP) stop layer.

17. The process of Claim 16, further comprising:

forming a layer of light-sensitive material on said layer of TERA material, wherein the optical properties of said light-sensitive layer and said TERA layer are substantially the same;

and

exposing said layer of light-sensitive material to a pattern of radiation,

wherein said forming said layer of TERA material facilitates producing a pattern in said layer of light-sensitive material substantially the same as said pattern of radiation.

18. The process of claim 17, wherein said forming said layer of TERA material comprises providing a part of the lithographic structure for the formation of a metal interconnect for said device structure.

19. The process of claim 17, wherein said forming said layer of TERA material comprises depositing said layer of TERA material using at least one of chemical vapor deposition (CVD), and plasma enhanced CVD.

20. The process of Claim 16, wherein said forming a damascene structure comprises integrating a tunable anti-reflective coating with a single damascene structure.

21. The process of Claim 16, wherein said forming a damascene structure comprises integrating a tunable anti-reflective coating with a dual damascene structure.

22. The process of Claim 21, wherein said forming a damascene structure comprises integrating a tunable anti-reflective coating with a dual damascene structure formed using a method comprising at least one a via-

first method, a full-via-first method, a full-via with no stop layer method, a trench-first method, and a buried via mask method.

23. A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a second dielectric layer formed on said first dielectic layer, a hard mask layer formed on said dielectric layer, a tunable etch resistant anti-reflective (TERA) coating formed on said hard mask layer, and a first layer of light-sensitive material formed on said TERA coating;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said TERA coating;

forming a second layer of light-sensitive material on said TERA coating;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said TERA coating;

transferring said first pattern to said hard mask layer;

transferring said first pattern to said second dielectric layer;

transferring said second pattern to said hard mask layer;

transferring said second pattern to said second dielectric layer;

transferring said first pattern to said first dielectric layer; and

transferring said first pattern to said metal cap layer.

24. The method of claim 23, further comprising:

removing said first layer of light-sensitive material.

25. The method of claim 23, further comprising:

removing said second layer of light-sensitive material.

26. The method of claim 23, further comprising:

preparing said film stack with an etch stop layer formed on said first dielectric layer prior to said second dielectric layer formed on said etch stop layer; and

transferring said first pattern to said etch stop layer.

27. The method of claim 23, further comprising:

forming a layer of bottom anti-reflective coating (BARC) on said TERA coating; and

removing said BARC layer.

28. A semiconductor device comprising:

a semiconductor substrate;

a film stack formed on the semiconductor substrate; and

means for integrating a tunable anti-reflective coating with a damascene structure for a metal interconnect formed in the film stack.

29. A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a second dielectric layer formed on said first dielectric layer, a hard mask layer formed on said dielectric layer, a first tunable etch resistant anti-reflective (TERA) coating formed on said hard mask layer, a second TERA coating formed on said first TERA coating, and a first layer of light-sensitive material formed on said TERA coating;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said second TERA coating;

forming a second layer of light-sensitive material on said TERA coating;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said first TERA coating;

transferring said second pattern to said hard mask layer;

transferring said second pattern to said second dielectric layer;

transferring said second pattern to said first dielectric layer;

transferring said first pattern to said first TERA coating;

transferring said first pattern to said hard mask layer;

transferring said first pattern to said second dielectric layer; and

transferring said second pattern to said metal cap layer.

30. The method of claim 29, further comprising:

removing said first layer of light-sensitive material following said transferring said first pattern to said second TERA coating.

31. The method of claims 29, or 30, further comprising:

removing said second layer of light-sensitive material following said transferring said second pattern to said second dielectric layer.

32. The method of claims 29, 30, or 31, further comprising:

preparing said film stack with an etch stop layer formed on said first dielectric layer prior to said second dielectric layer formed on said etch stop layer; and

transferring said second pattern to said etch stop layer.

33. A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a tunable etch resistant anti-reflective (TERA) coating formed on said first dielectric layer, and a first layer of light-sensitive material formed on said TERA coating;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said TERA coating;

forming a second dielectric layer on said TERA coating;

forming a second TERA coating on said film stack;

forming a second layer of light-sensitive material on said second TERA coating;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said second TERA coating;

transferring said second pattern to said second dielectric layer;

transferring said first pattern to said first dielectric layer; and

transferring said first pattern to said metal cap layer.

34. The method of claim 33, further comprising:

forming a hard mask layer on said second dielectric layer; and

forming said second TERA coating on said hard mask layer; and

transferring said second pattern to said hard mask layer.

35. A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a hard mask formed on said first dielectric layer, a tunable etch resistant anti-reflective (TERA) coating formed on said hard mask layer, and a first layer of light-sensitive material formed on said TERA coating;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said TERA coating;

transferring said first pattern to said hard mask layer;

transferring said first pattern to said first dielectric layer;

transferring said first pattern to said metal cap layer;

removing said TERA coating;

filling said first pattern in said first dielectric layer and said metal cap layer with metal;

forming a second metal cap layer on said film stack;

forming a second dielectric layer on said second metal cap layer;

forming a second hard mask layer on said second dielectric layer;

forming a second TERA coating on said second hard mask layer;

forming a second layer of light-sensitive material on said second TERA coating;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said second TERA coating;

transferring said second pattern to said second hard mask layer;

transferring said second pattern to said second dielectric layer; and

transferring said second pattern to said second metal cap layer.